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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,083	06/28/2001	Petruzzello John	US 010320	5332

7590

06/26/2002

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EXAMINER

SEFER, AHMED N

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 06/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/894,083

Applicant(s)

JOHN ET AL.

Examiner

A. Sefer

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-9, 15 and 16) in Paper No. 6 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Momose et al. US Patent No. 5,990,516.

Momose et al disclose in fig. 28 a hybrid semiconductor device, comprising a first portion 9 or a MOSFET transistor (as in claim 2) being relatively resistant to breakdown; and a second portion 11 or a diode (as in claim 3) being less resistant to breakdown.

As to claim 4, Momose et al disclose a first portion comprising a MOS transistor and a second portion comprising a diode.

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As to claim 6, Momose et al disclose breakdown occurs at higher voltage in the first portion, and at a lower voltage in the second portion.

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Letavic et al. US Patent No. 6,133, 591.

Letavic et al disclose (see col. 4, lines 27-51) a hybrid semiconductor device, comprising a first portion (see fig. 3) or a MOSFET transistor (as in claim 2) being relatively resistant to breakdown; and a second portion (see fig. 2) comprising diode (as in claim 3) being less resistant to breakdown.

As to claim 4, Letavic et al disclose a first portion comprising a MOS transistor and a second portion comprising a diode.

As to claim 5, Letavic et al disclose a diode (see fig. 3) having identical structure as MOS transistor, except for a source region.

As to claim 6, Letavic et al disclose breakdown occurs at higher voltage in the first portion, and at a lower voltage in the second portion.

5. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kouno et al. US Patent 6,365,932.

Kouno et al disclose (see fig. 3 and col. 9, lines 24-34) a hybrid semiconductor device, comprising a first portion or a MOSFET transistor (as in claim 2) being relatively resistant to breakdown; and a second portion D1 or a diode (as in claim 3) being less resistant to breakdown.

As to claim 4, Kouno et al disclose a first portion comprising a MOS transistor and a second portion comprising a diode.

As to claim 6, Kouno et al disclose breakdown occurs at higher voltage in the first portion, and at a lower voltage in the second portion.

6. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Kamei et al. (JP 2000-260883).

Kamei et al disclose in fig. 3 a hybrid semiconductor device, comprising a first portion 26 or a MOSFET transistor (as in claim 2) being relatively resistant to breakdown; and a second portion 22 or a diode (as in claim 3) being less resistant to breakdown.

As to claim 4, Kamei et al disclose a first portion comprising a MOS transistor and a second portion comprising a diode.

As to claim 6, Kamei et al disclose breakdown occurs at higher voltage in the first portion, and at a lower voltage in the second portion.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamei et al. (JP 2000-260883) in view of Letavic et al. US Patent No. 5,969,387.

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Kamei et al. disclose all the claimed subject matter except a diode having an identical structure as a MOS transistor, except for a source region.

Latevic et al. disclose a diode (fig. 3) having an identical structure as a MOS transistor except for a source region.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Latevic et al with Kamei et al, since that would provide identical fabrication steps.

9. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Letavic et al. US Patent 6,133, 591 in view of Honda US Patent No. 5,834,823.

Letavic et al disclose all the claimed subject matter including an SOI-LDMOS device (as in claim 8) except a breakdown voltage due to a difference in field plate length.

Honda discloses (see figs. 1-4) a breakdown voltage differential due to a difference in field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Honda's teaching with Letavic et al, since that would provide an efficient high-voltage structure.

10. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno et al. US Patent 6,365,932 in view of Honda US Patent No. 5,834,823.

Kouno et al disclose all the claimed subject matter including an SOI-LDMOS device (as in claim 8) except a breakdown voltage due to a difference in field plate length.

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Honda discloses (see figs. 1-4) a breakdown voltage differential due to a difference in field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Honda's teaching with Letavic et al, since that would provide an efficient high-voltage structure.

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno et al. US Patent 6,365,932 in view of Pendharkar et al. US Patent No. 6,160,290.

Kouno et al disclose all the claimed subject matter including an SOI-LDMOS device (as in claim 8) except a breakdown voltage due to a difference in field plate length.

Pendharkar et al disclose (see figs. 1 and 2) a breakdown voltage differential due to a difference in field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Pendharkar with Letavic et al, since that would provide an efficient high-voltage structure.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Letavic et al. US Patent No. 6,133,591 in view of Honda.

Letavic et al disclose in figs. 2 and 3 a hybrid lateral thin-film silicon-on-insulator device comprising a first region comprising a semiconductor substrate 22, a buried insulating layer 24 on said substrate, and a lateral MOS device in an SOI layer on said buried insulating layer and a source region 28 of a first conductivity type formed in a body region 30 of a second conductivity type opposite to that of the first, a lateral drift

region 32 of said first conductivity type adjacent to said body region, a drain region 34 of first conductivity type and laterally spaced apart from said body region by said lateral drift region, a gate electrode 36 over a part of said body region and over a first part of said lateral drift region adjacent to body region, said gate electrode being insulated from said body region and drift region by a first insulation region 38, with a field plate 36A comprised of conducting material extending laterally over said lateral drift region and being electrically connected to said gate electrode; and one or more second regions integrated with the first region, said second regions being identical to the first region, except not comprising said source region (see fig. 3).

Honda discloses (see figs. 1-4) the use of shorter/longer field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ a field plate of shorter length with the second region than that of first region, since that would provide an efficient high-voltage structure.

13. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Letavic et al. US Patent No. 5,969,387 in view Honda.

Letavic et al disclose in figs. 1-3 a hybrid lateral thin-film silicon-on-insulator device comprising a first region comprising a semiconductor substrate 100, a buried insulating layer 102 on said substrate, and a lateral MOS device in an SOI layer on said buried insulating layer and a source region 116 of a first conductivity type formed in a body region 106 of a second conductivity type opposite to that of the first, a lateral drift region 110 of said first conductivity type adjacent to said body region, a drain region 108 of first conductivity type and laterally spaced apart from said body region by said lateral

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drift region, a gate electrode 114 over a part of said body region and over a first part of said lateral drift region adjacent to body region, said gate electrode being insulated from said body region and drift region by a first insulation region 112, with a field plate 114A comprised of conducting material extending laterally over said lateral drift region and being electrically connected to said gate electrode; and one or more second regions integrated with the first region, said second regions being identical to the first region, except not comprising said source region (see fig. 3).

Honda discloses (see figs. 1-4) the use of shorter/longer field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ a field plate of shorter length with the second region than that of first region, since that would provide an efficient high-voltage structure.

As to claim 16, Letavic et al disclose that the width of a second region at least as long as a lateral drift region.

14. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Letavic et al. US Patent No. 5,969,387 in view Pendharkar et al.

Letavic et al disclose in figs. 1-3 a hybrid lateral thin-film silicon-on-insulator device comprising a first region comprising a semiconductor substrate 100, a buried insulating layer 102 on said substrate, and a lateral MOS device in an SOI layer on said buried insulating layer and a source region 116 of a first conductivity type formed in a body region 106 of a second conductivity type opposite to that of the first, a lateral drift region 110 of said first conductivity type adjacent to said body region, a drain region 108 of first conductivity type and laterally spaced apart from said body region by said lateral

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drift region, a gate electrode 114 over a part of said body region and over a first part of said lateral drift region adjacent to body region, said gate electrode being insulated from said body region and drift region by a first insulation region 112, with a field plate 114A comprised of conducting material extending laterally over said lateral drift region and being electrically connected to said gate electrode; and one or more second regions integrated with the first region, said second regions being identical to the first region, except not comprising said source region (see fig. 3).

Pendharkar et al disclose (see figs. 1 and 2) the use of shorter/longer field plate length.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ a field plate of shorter length with the second region than that of first region, since that would provide an efficient high-voltage structure.

As to claim 16, Letavic et al disclose that the width of a second region at least as long as a lateral drift region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

AND
June 21, 2002

NATHAN J. FLYNN
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